**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claims 1-15 (canceled).

16. (New) A program-controlled computer unit, comprising:

a single controller core including at least a first execution unit and a second execution unit;

wherein the first and the second execution units are operable independently of one another in a first operating mode, and wherein the first and the second execution units are operable in a second operating mode to process the same set of instructions in parallel.

17. (New) The program-controlled computer unit as recited in Claim 16, further comprising:

an error detection device that performs, in the second operating mode, at least one of an error detection and an error correction in accordance with an error handling routine.

18. (New) The program-controlled computer unit as recited in Claim 17, wherein the error detection device includes a coder that provides at least one of: a) an error detection code to input data conveyed to the first and the second execution units on the input side; and b) an error correction code to an output signal calculated by at least one of the first and the second execution units.

19. (New) The program-controlled computer unit as recited in Claim 18, wherein the error detection device includes a first comparison unit downstream from the first and the second execution units on the output side, and wherein the first comparison unit provides a comparison, in accordance with an error handling routine, for at least one of the following: a) a set of output signals calculated by the first and the second execution units; and b) a set of error correction codes assigned to output signals calculated by the first and the second execution units, whereby it is determined whether an error is present, and wherein an error signal is output in the event an error is present.

20. (New) The program-controlled computer unit as recited in Claim 19, wherein the error detection device includes a second comparison unit upstream from at least one of the first and the second execution units on the input side, the second comparison unit comparing input data conveyed to at least one of the first and the second execution units on the input side with input data provided with a checksum, in accordance with an error detection routine, to determine whether an error is present, and wherein an error signal is output in the event an error is present.

21. (New) The program-controlled computer unit as recited in Claim 20, further comprising:

at least one data register associated with at least one of the first and the second execution units, wherein the at least one data register is connected on the output side to both the inputs of the first and the second execution units and to the second comparison unit, and wherein input data for at least one of the first and the second execution units are stored in the at least one data register.

22. (New) The program-controlled computer unit as recited in Claim 20, further comprising:

a shadow register, wherein input data most recently conveyed to at least one of the first and the second execution units prior to calculation are stored.

23. (New) The program-controlled computer unit as recited in Claim 22, wherein the shadow register is a first-in-first-out register.

24. (New) The program-controlled computer unit as recited in Claim 22, further comprising:

a control device coupled on the input side to the error detection device and coupled on the output side to the shadow register, wherein the control device generates an enabling signal for enabling the shadow register only if no error is detected by the error detection device.

25. (New) The program-controlled computer unit as recited in Claim 24, wherein the program-controlled computer unit is one of a microcontroller and a microprocessor.

26. (New) A method for operating a program-controlled computer unit that includes: a) a single controller core having at least a first execution unit and a second execution unit, wherein the first and the second execution units are operable independently of one another in a first operating mode, and wherein the first and the second execution units are operable in a second operating mode to process the same set of instructions in parallel; and b) an error detection

device having at least one comparison unit, the method comprising:

performing, in the second operating mode, at least one of an error detection and an error correction in accordance with an error handling routine using the error detection device, wherein the at least one comparison unit provides a comparison, accordance with an error handling routine, for at least one of the following: a) a set of input data for the first and the second execution units; b) a set of output signals calculated by the first and the second execution units; and c) a set of error correction codes assigned to output signals calculated by the first and the second execution units, and wherein an error signal is generated if the comparison does not produce an agreement.

27. (New) The method as recited in Claim 26, wherein different error signals are generated for different types of error.

28. (New) The method as recited in Claim 27, wherein the input data are first conveyed to both the first and the second execution units, and subsequently corresponding error correction codes are generated from the input data.

29. (New) The method as recited in Claim 28, wherein stored input data of the previous calculation are overwritten only if one of: a) a comparison of the stored input data; and b) a comparison of output result data calculated from the stored input data, does not result in an error signal.

30. (New) The method as recited in Claim 29, wherein the output result data calculated from the stored input data are transmitted for only if an error signal is not present.